The silicon industry: Career paths and research opportunities

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University of Dayton

Outline

- The silicon industry yesterday and today
- Semiconductor device fundamentals
- Semiconductor device fabrication and CMOS processing
- The Semiconductor Electronics and Photonics REU program at UD

What are semiconductors?

Insulators
glass
plastics
diamond

Semiconductors
silicon
germanium
gallium arsenide

Conductors
metals
transparent conducting oxides

low — high

Electrical conductivity

Properties of crystalline semiconductors

- Moderate intrinsic conduction
- Conductivity controlled by addition of impurities (*p*-type, *n*-type) – **doping**
- Can be used in conjunction with metals and oxides to create diodes (*p*-*n* junctions), transistors (MOSFET, JFET, BJT), resistors, and capacitors
- Optical absorption of photons with energy above band gap, can be used to create photodetectors

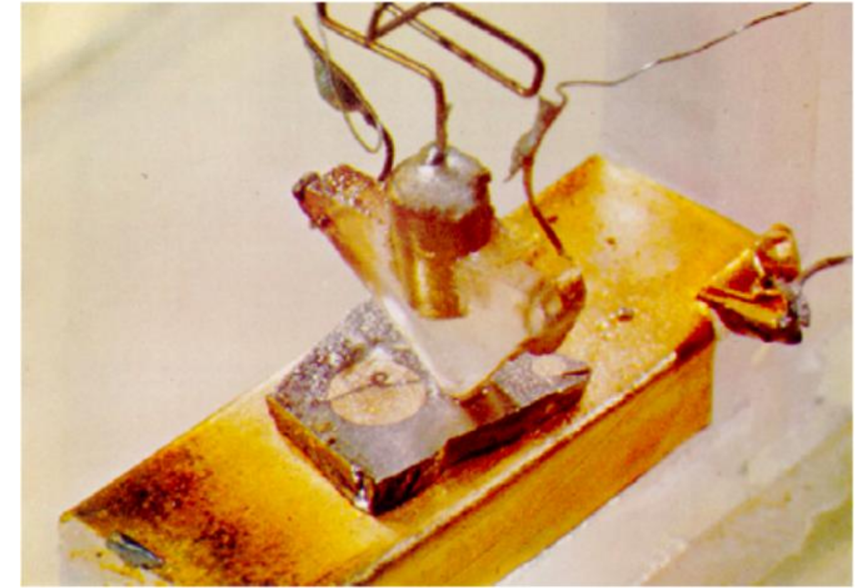
A little history

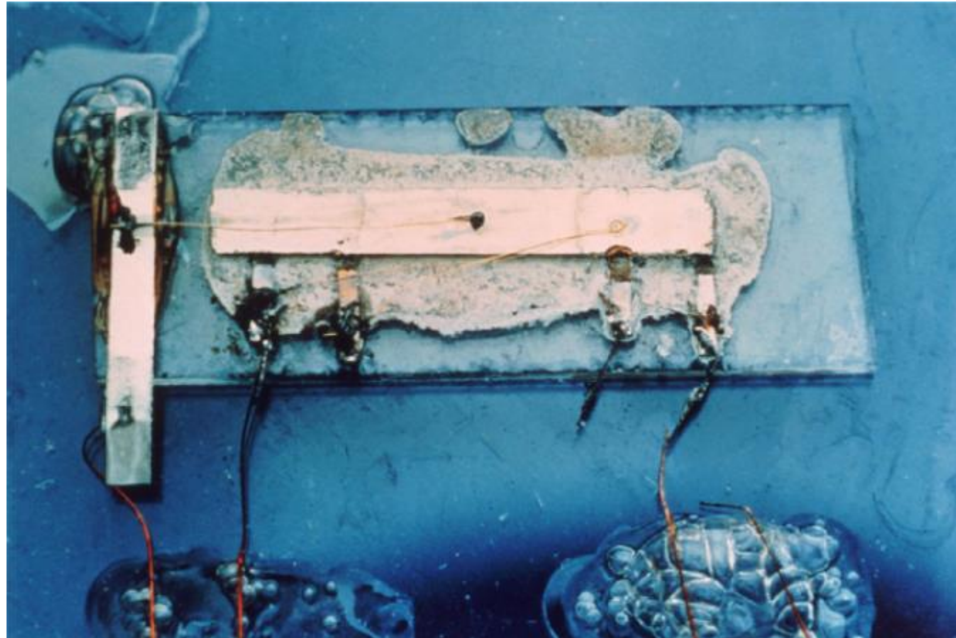
1942: First high-purity semiconductor (Lark-Horovitz, Purdue)

1947: Point contact transistor (Bardeen & Brattain at Bell Labs)

1951: Junction transistor (Teal & Sparks at Bell Labs)

1955: Photolithography and diffusion





1956: Shockley moves to CA to start Shockley Semiconductor

1960: First MOSFET (Atalla & Kahng at Bell Labs)

1963: Standard logic ICs

1965: Moore's law predicts future

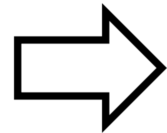
Above: Picture of the first point-contact transistor created by Bardeen and Brattain at Bell Labs
Left: Picture of first integrated circuit created by Kilby at Fairchild Semiconductor

The shift to silicon

In order to create mass manufacturing, the world needed to pool its resources and concentrate on one material: Silicon

Possibilities

- Germanium
- **Silicon**
- Gallium Arsenide



Why Si?

- Earth abundant material
- Non-toxic
- Reasonably low conductivity at room temp
- Native oxide is SiO_2, which is very stable and a good insulator

The silicon industry today

Today

- **$590bn** worldwide industry as of 2021
- Microprocessors integrated into our daily lives
- Society dependent on semiconductors

Current research areas

- Reducing transistor size
- New materials
- Silicon photonics
- Biological applications

My research area: Silicon photonics

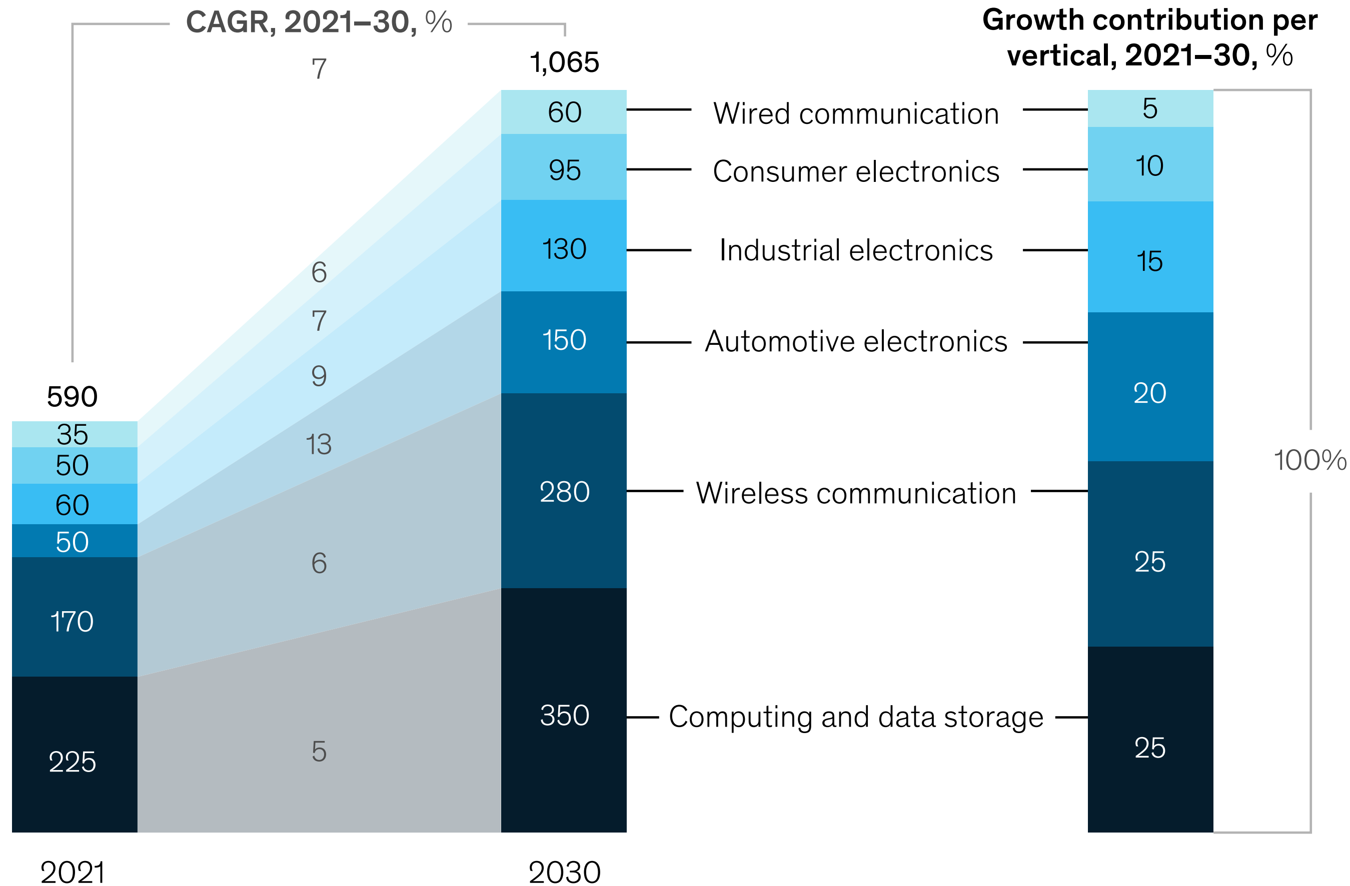
Transistor count

Year in which the microchip was first introduced

Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

Figure: Plot of number of transistors per microprocessor as a function of time.

A growing industry



$590 bn in 2021

$1,065 bn in 2030 projected

Over 1 trillion dollars

Biggest growth areas:

- Automotive electronics
- Wireless communication
- Computing and data storage

Semiconductor device fundamentals

Doping of semiconductors

Doping during wafer fabrication

Dopants can be introduced into the liquid semiconductor prior to the Czochralski or float zone growth method.

Ion implantation + annealing

Wafer is bombarded with a beam of ions of the desired dopant atom. Any exposed areas will be implanted with dopant atoms. Requires post-implantation annealing.

Diffusion doping

Wafer is placed in a furnace and heated to high temperature in the presence of a gas with the desired dopant atom. Dopant will diffuse into any exposed portions of the wafer.

Doping during thin film growth

Dopants can be introduced as gases or solids during thin film growth processes such as CVD, MBE, and magnetron sputtering.

Silicon dopants

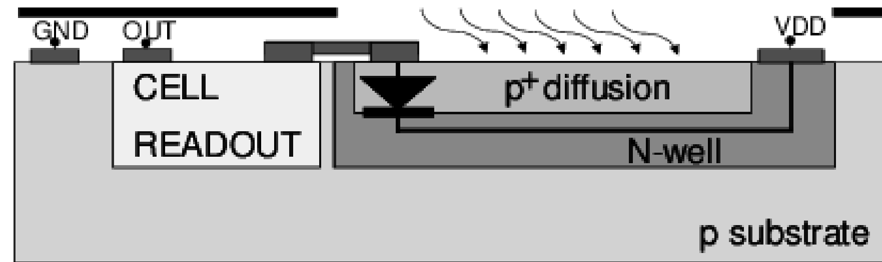
p-type
Group III
--B, Al, Ga

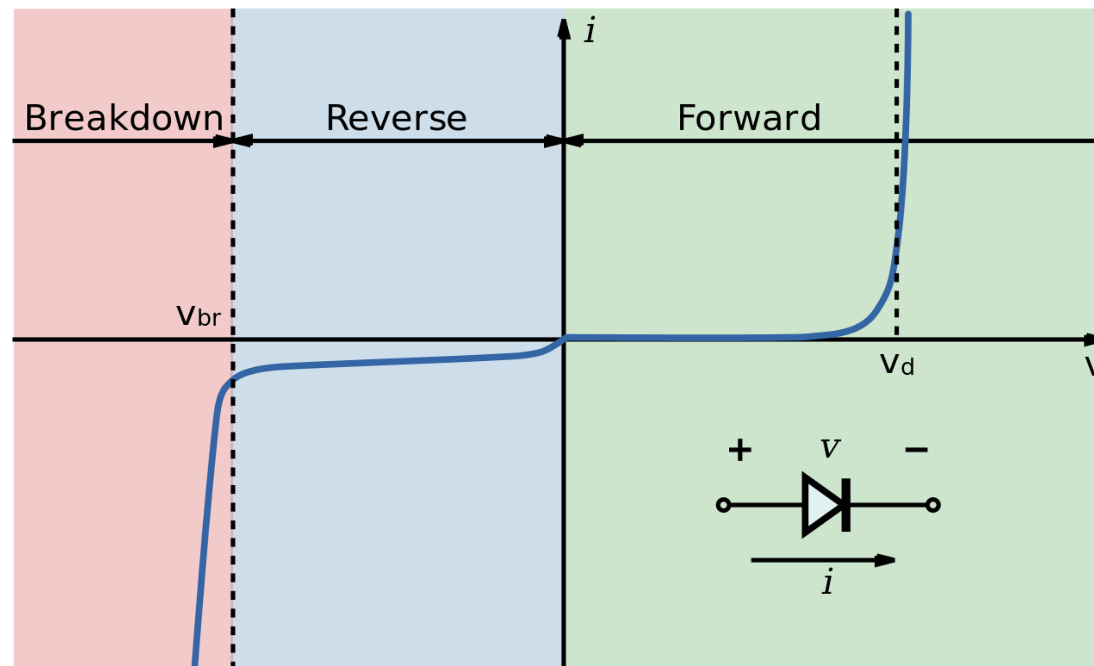
n-type
Group Va
--P, As, Sb

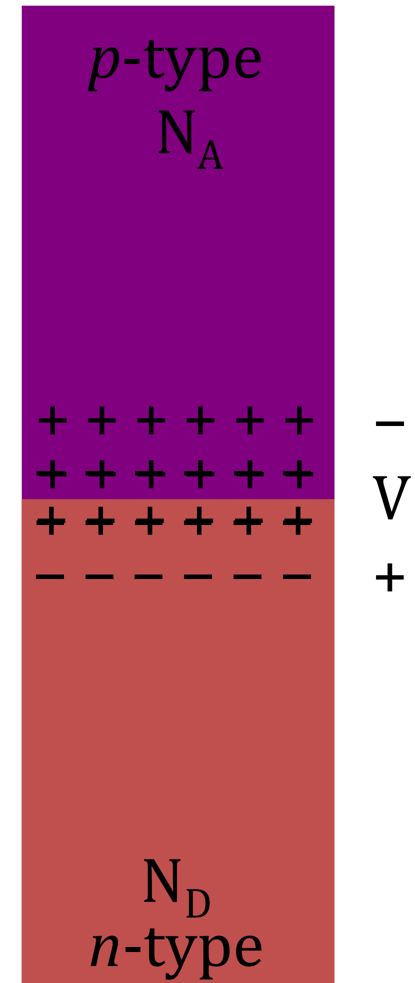
3A	4A	5A
5 B $1s^22s^2p^1$	6 C $1s^22s^2p^2$	7 N $1s^22s^2p^3$
13 Al [Ne]$3s^2p^1$	14 Si [Ne]$3s^2p^2$	15 P [Ne]$3s^2p^3$
31 Ga [Ar]$3d^{10}4s^2p^1$	32 Ge [Ar]$3d^{10}4s^2p^2$	33 As [Ar]$3d^{10}4s^2p^3$
49 In [Kr]$4d^{10}5s^2p^1$	50 Sn [Kr]$4d^{10}5s^2p^2$	51 Sb [Kr]$4d^{10}5s^2p^3$
81	82	83

PN Junctions: Overview

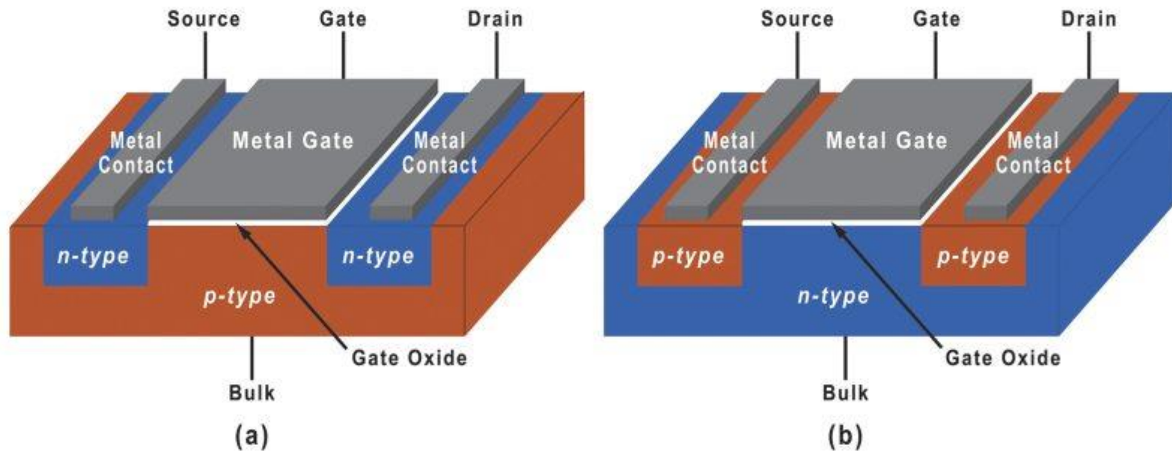
- When the junction is first formed, due to the concentration gradient electrons leave n-type region and holes leave p-type region
- Where they meet the electrons and holes annihilate each other to form the **depletion region**
- Due to charge transfer, a voltage difference occurs between regions
- This also results in **nonlinear current-voltage behavior**

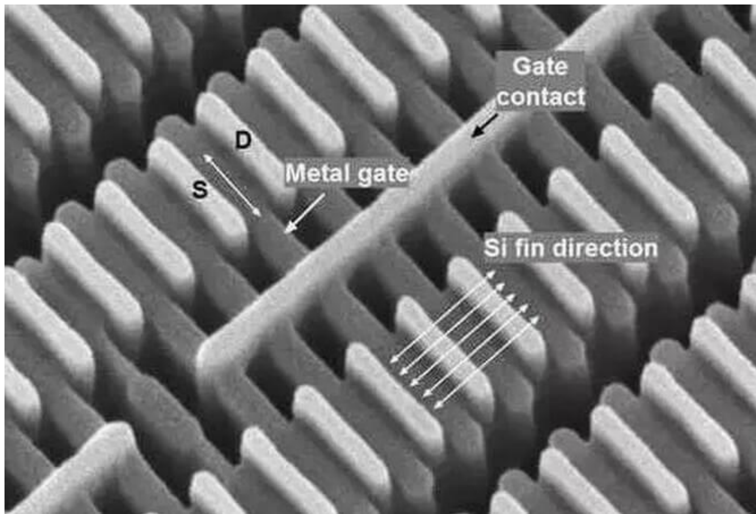


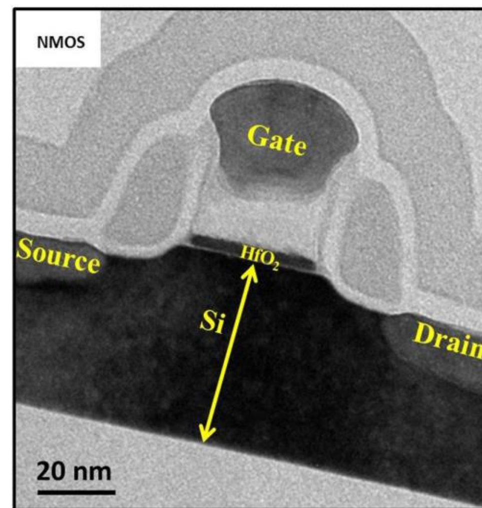




The most common device: MOSFET





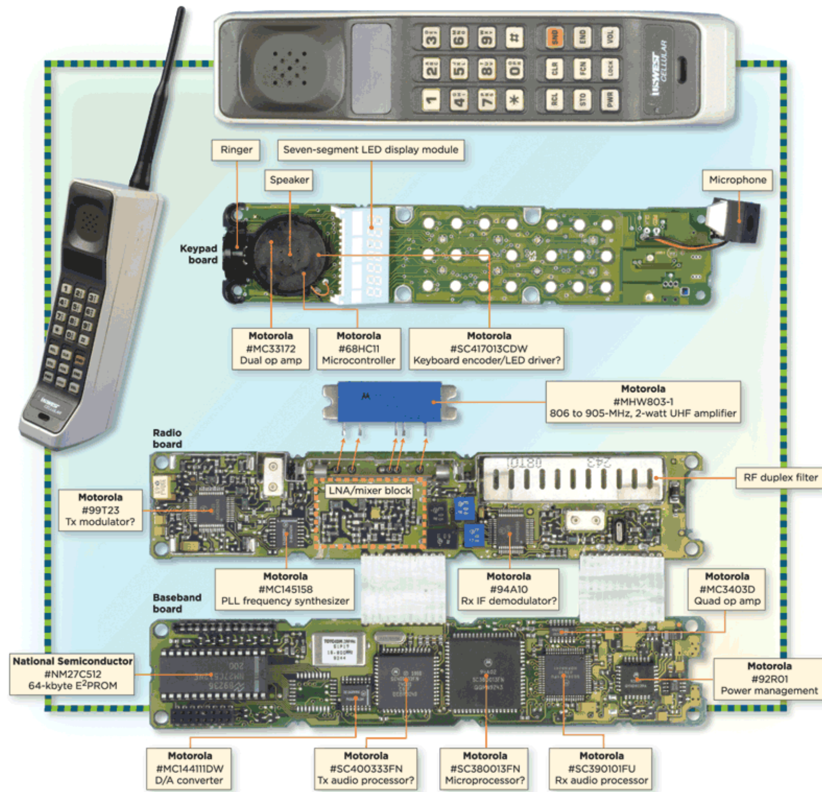


- Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
- Can operate like a voltage-controlled switch
- Chained together to form logic gates (AND, OR, NAND, etc.)
- Microprocessors have many logic gates
- Can also be used to build amplifiers

Mass manufacturing of integrated circuits

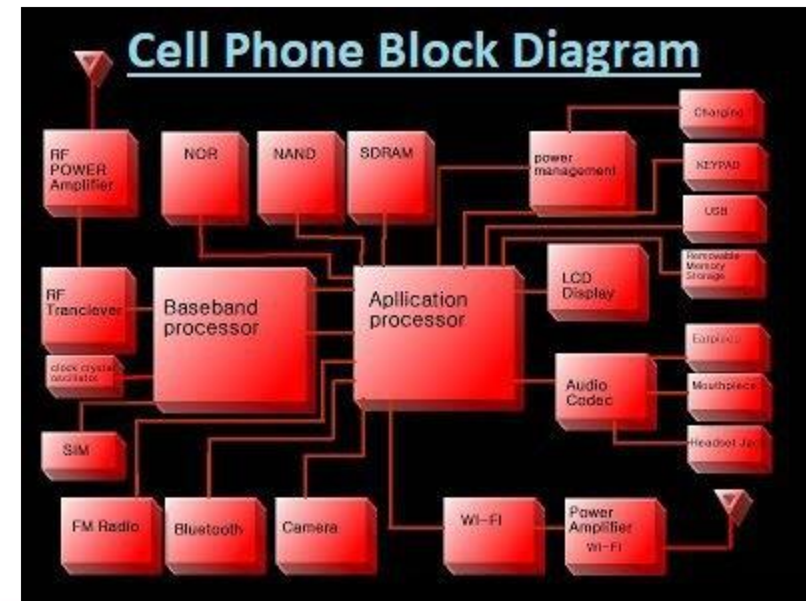
Traditional electronics

- Individual components or small circuits with different functions fabricated and packaged separately
- Components connected with wires or on a circuit board



Integrated electronics

- Components or small circuits of all types are created on the same chip
- Components are connected by metal lines formed through lithography and deposition
- Many components can be fabricated simultaneously
- Chip only needs one package and interface



Semiconductor device fabrication and complementary metal-oxide-semiconductor (CMOS) processing

The Clean Room environment

Today's MOSFETs have sizes down to 4 nm, which is 5 orders of magnitude smaller than the width of a hair. To successfully make these chips we need a clean room.

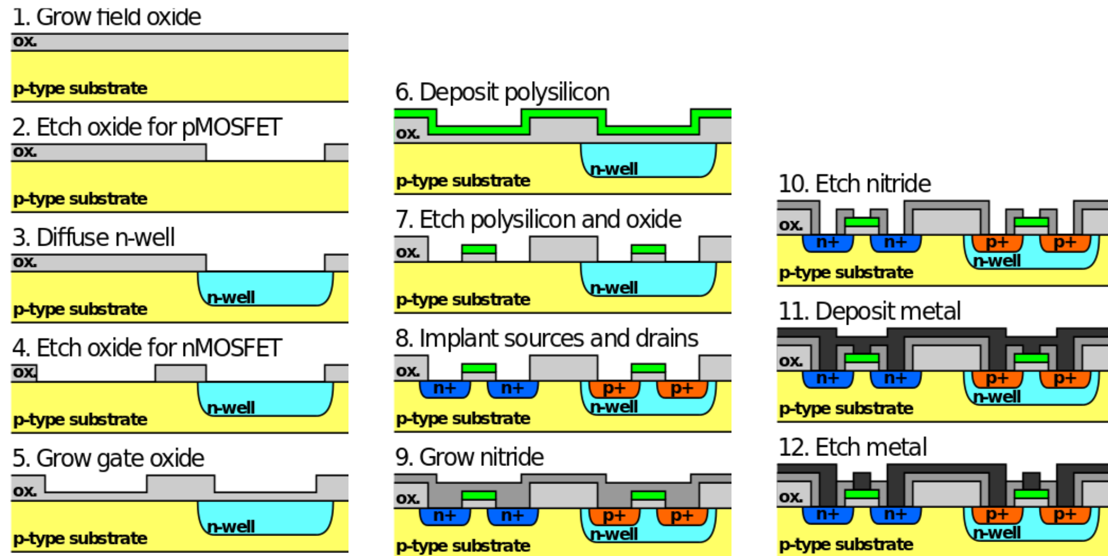
Clean room facts

- Air is heavily filtered to remove dust particles and impurities
- Humidity and temperature strictly controlled
- Constant laminar air flow from top to bottom
- Workers wear clean room garments to cover all areas to protect devices and for safety
- Strict protocols on gowning, safety, chemical handling, and tool use

The Complementery Metal-Oxide-Semiconductor process

Integrated circuit fabrication is a series of steps to define devices that are mostly planar

Lithography is used to create patterns to define areas for doping, selective etching, or selective material deposition



- Device and circuit design
- Layout and masks
- Start with Si wafer
- Lithograpy to create patterns
- Doping to create *p*- and *n*-type
- Deposition of materials
- Etching of materials
- Metrology and testing
- Packaging

Mass manufacturing of integrated circuits

Wafers are 8”, 12”, or 18”, carried in cassettes

Tools are automated and have internal clean room environments

Workers operate tools programmatically

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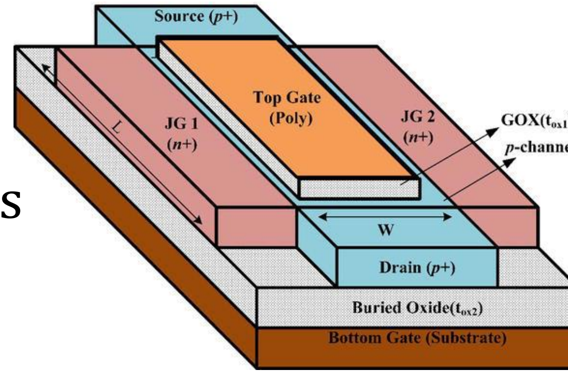
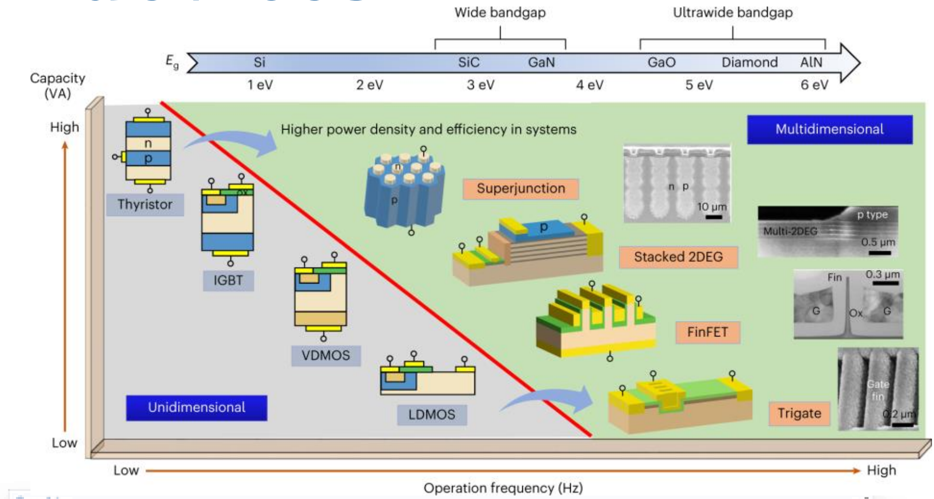
Design of semiconductor devices

Design needs:

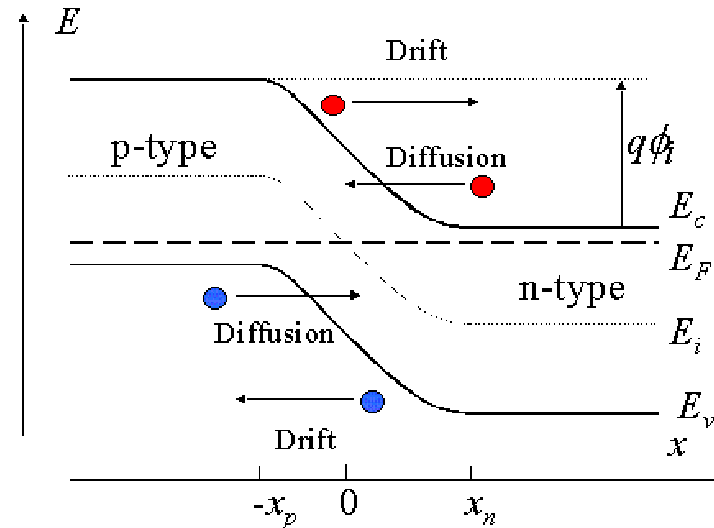
- New device architectures
- Improving device performance
- Making devices with new materials
- Ohmic contact formation
- Computer modeling of devices

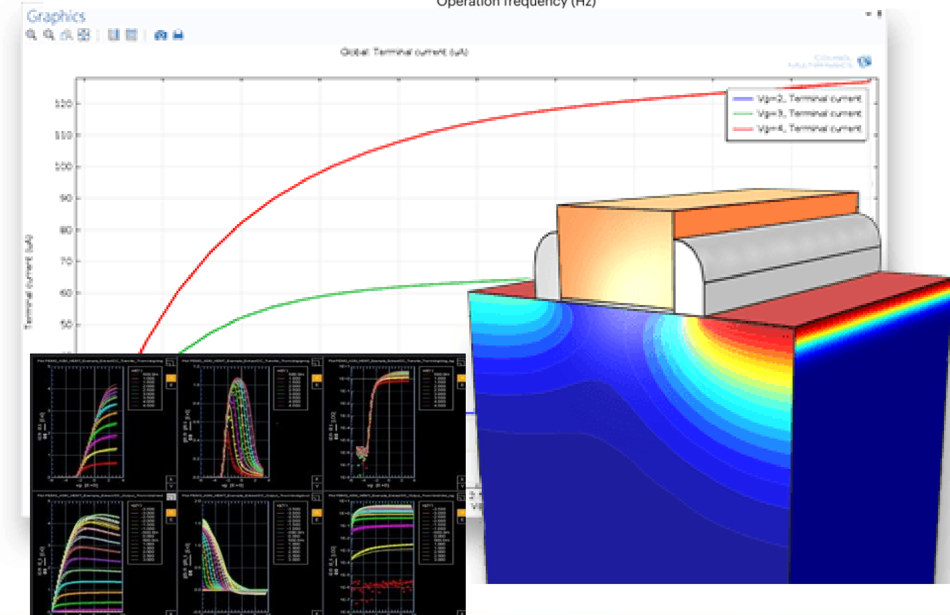




Relevant majors

- Physics
- Electrical engineering
- Materials science and engineering





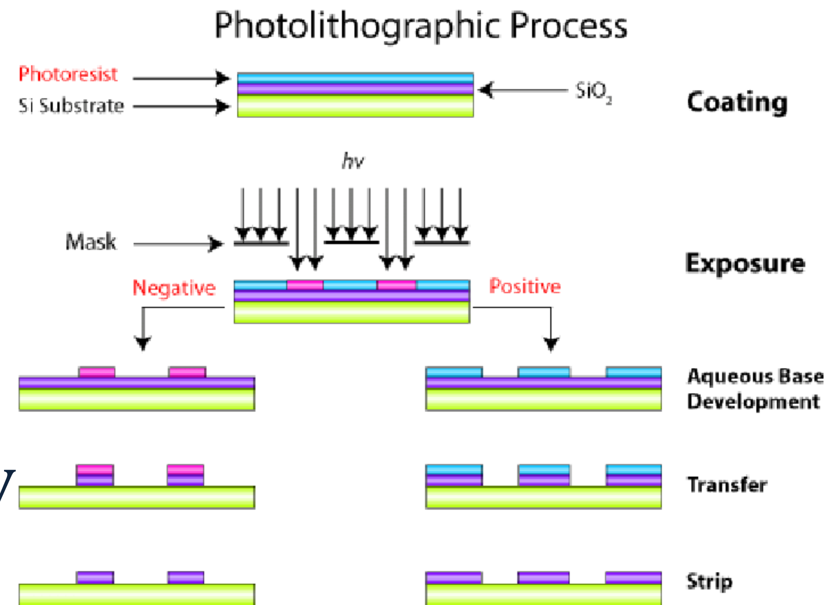
Defining patterns: Lithography

Lithography general process

- Photosensitive polymer material called photoresist is deposited using a spin coater then baked.
- Patterns are formed by selectively exposing the photoresist to light or electrons.
- Wafer is immersed in solvent that removes exposed (or unexposed) areas.
- Remaining photoresist is baked to dry and form a hard mask for diffusion, etching, or deposition of other materials.

Methods

- UV contact lithography
- Stepper lithography
- Direct write
- Electron-beam lithography
- Nanoscribe



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- Electrical engineering
- Chemistry
- Chemical engineering
- Materials science and engineering

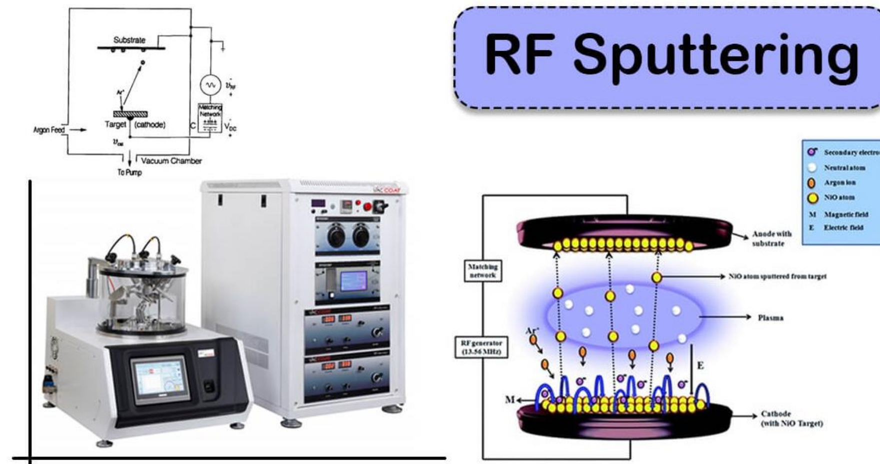
Deposition of metals, semiconductors, and dielectrics

Deposition methods

- **Magnetron sputtering** – Ion beam is used to ablate material from a target onto the wafer under vacuum.
- **Thermal evaporation** – Solid material is heated under vacuum and evaporated using resistive heating.
- **Electron beam evaporation** – Small crucible of solid material is heated under vacuum and evaporated using an electron beam.
- **Chemical vapor deposition (CVD)** – Wafer is placed in a vacuum chamber and reactive gases are introduced, causing a chemical reaction at the wafer surface that forms a solid material.
- **Plasma-enhanced chemical vapor deposition (PECVD)** – Similar to CVD but with the addition of a plasma at the wafer surface to increase reactivity and growth rates.
- **Molecular beam epitaxy (MBE)** – Solid materials are heated under vacuum and directed to the wafer surface to form solid material. Requires UHV and has low growth rates.
- **Atomic layer deposition (ALD)** – Wafer is under vacuum and is repeatedly introduced to small amounts of gases one short cycle at a time to create single atomic layers of material.

Materials

- Metals – Cu, Au, Ti, Ag, V, etc.
- Oxides – SiO_2, HfO_2, ITO
- Nitrides – Si_3N_4
- Crystalline semiconductors – Si, Ge, SiGe, GeSn
- Amorphous semiconductors – a-Si



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- Chemical engineering
- Materials science and engineering
- Mechanical engineering

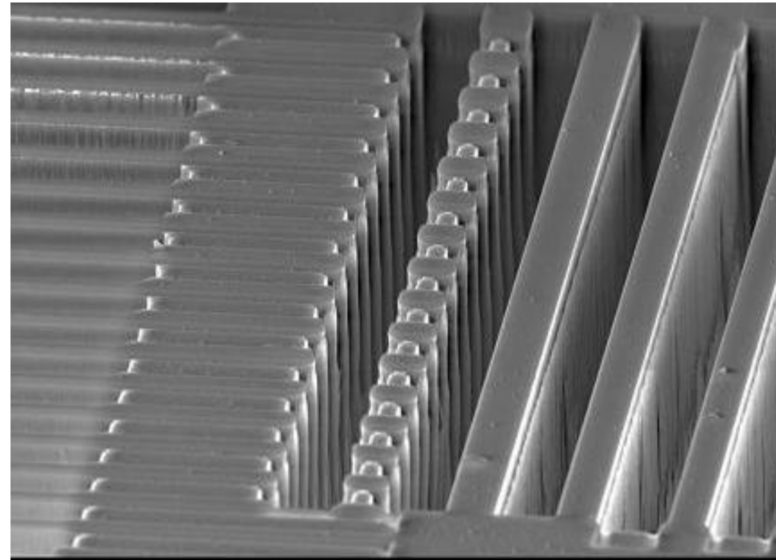
Making structures: Etching of materials

The etch process

- Once pattern is formed using lithography, materials can be etched away
- Plasma etchers (RIE or ICP) use gases in a vacuum chamber to etch material
- Wet etching uses liquid chemicals
- Etch is performed until the desired depth has been reached

Methods

- Reactive ion etching
- Inductively-coupled plasma etching
- Wet etching
- Ion beam milling



Relevant majors

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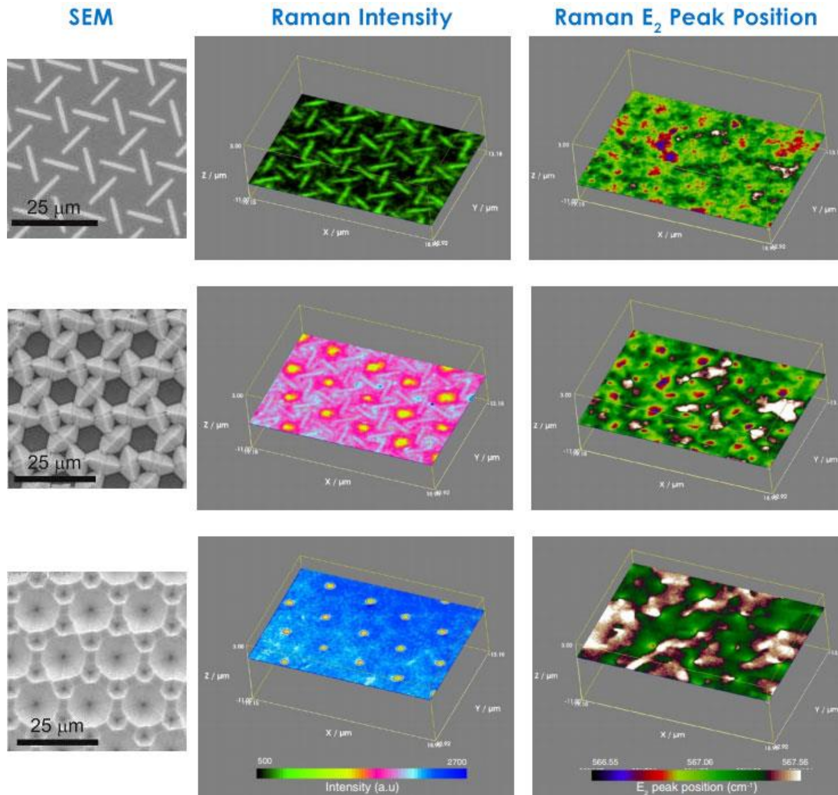
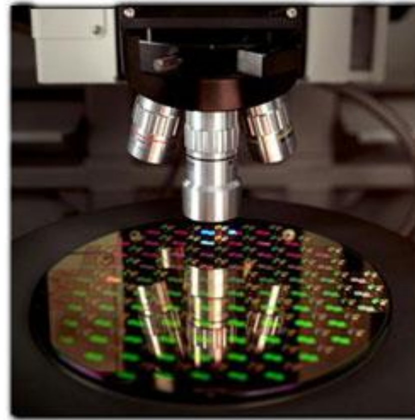
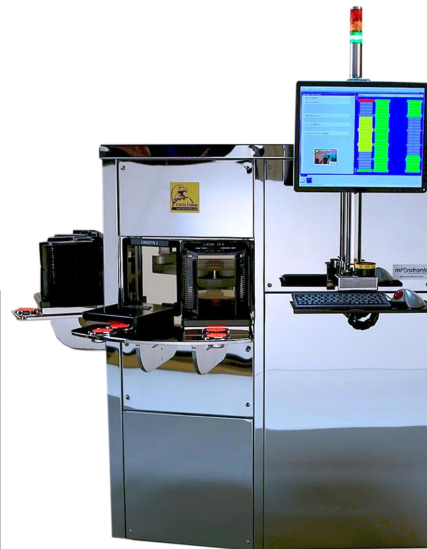
Metrology

During fabrication there are many measurements to check the results of the various process steps







Relevant majors

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- Chemistry
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- Mechanical engineering

Characterization techniques

- Optical microscopy – lithography, structure
- Scanning electron microscopy – structure
- X-ray diffraction (XRD) – crystallinity, strain
- Raman scattering – strain, composition
- Ellipsometry – film thickness, optical properties
- Profilometry – etch depth
- Atomic force microscopy – surface features
- Current-voltage – DC electrical response
- Capacitance-voltage – frequency response

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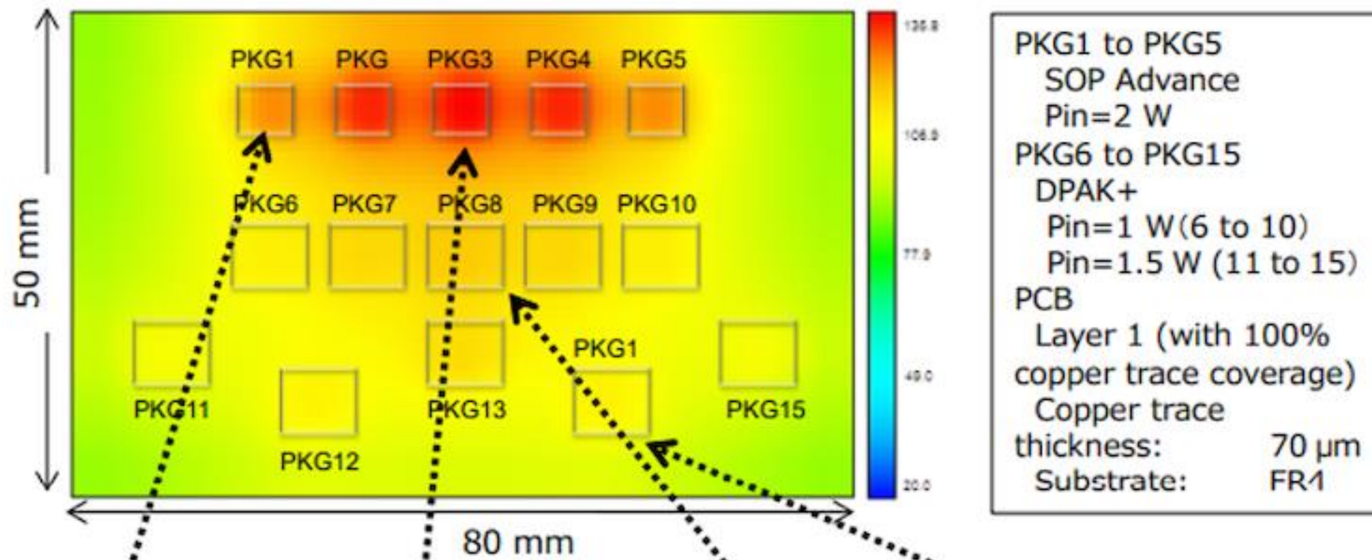
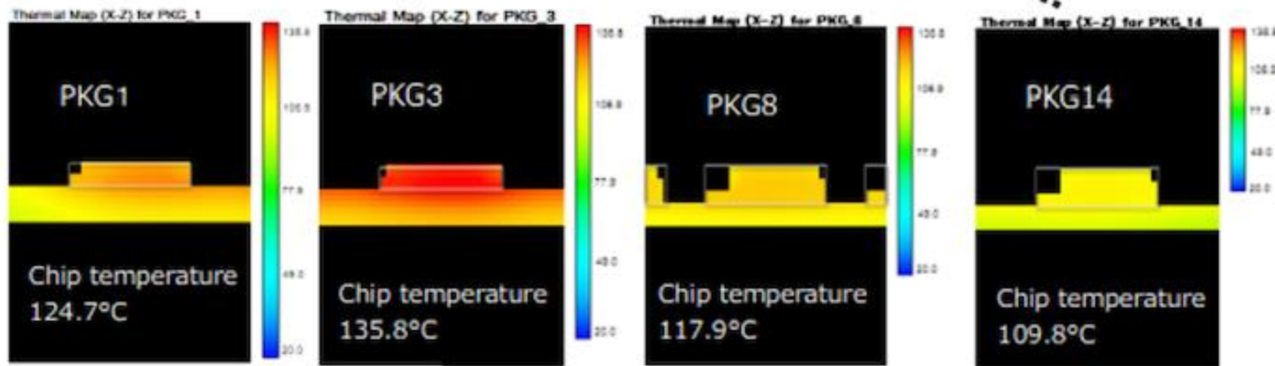
Packaging





Once the chip is fabricated, it has to be packaged for use on a circuit board. The package must be:

- Compact
- Physically robust
- Electrically-insulating
- Thermally-conductive

Relevant majors

- Physics
- Electrical engineering
- Materials science and engineering
- Mechanical engineering

Tools and equipment for fabrication

The tools for fabrication are complicated, precise, and expensive. There is an industry devoted to making these tools.

- Deposition chambers
- Plasma etchers
- Wet chemical tools
- Lithography tools
- Wafer probing
- Metrology tools
- Furnaces
- Automation and control
- Climate control

Relevant majors

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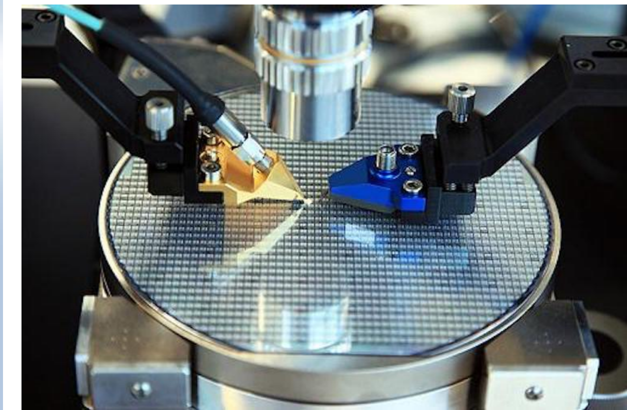
- Materials science and engineering
- Mechanical engineering
- Chemistry
- Chemical engineering



Safety and chemical handling

Semiconductor fabrication uses many hazardous chemicals, as well as vacuum chambers, high voltages, and other safety hazards.

- Chemical handling
- Hazardous waste disposal
- Chemical waste recycling
- Safety procedures and protocols
- Environmental controls

Relevant majors
- Chemistry
- Chemical engineering
- Environmental engineering
- Mechanical engineering
- Physics

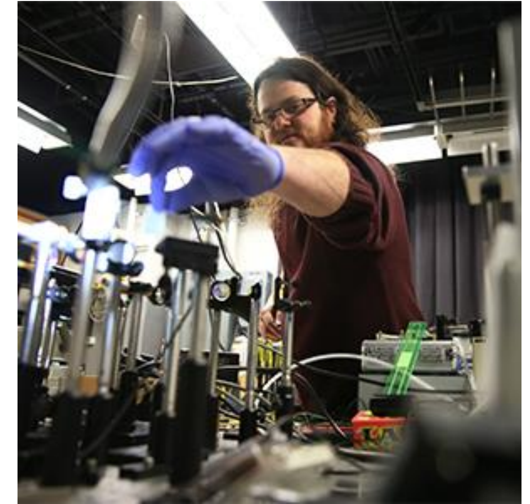
The REU in Semiconductor Electronics and Photonics at University of Dayton

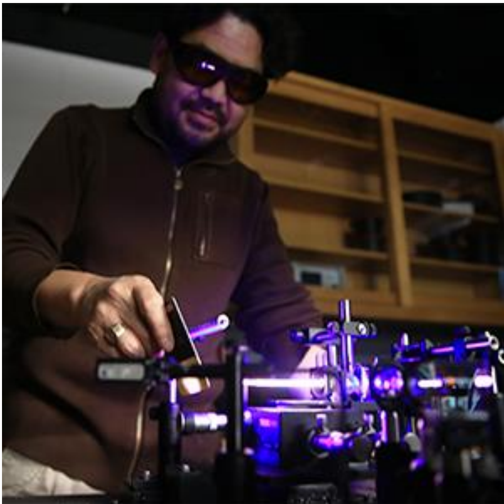
The Physics Department

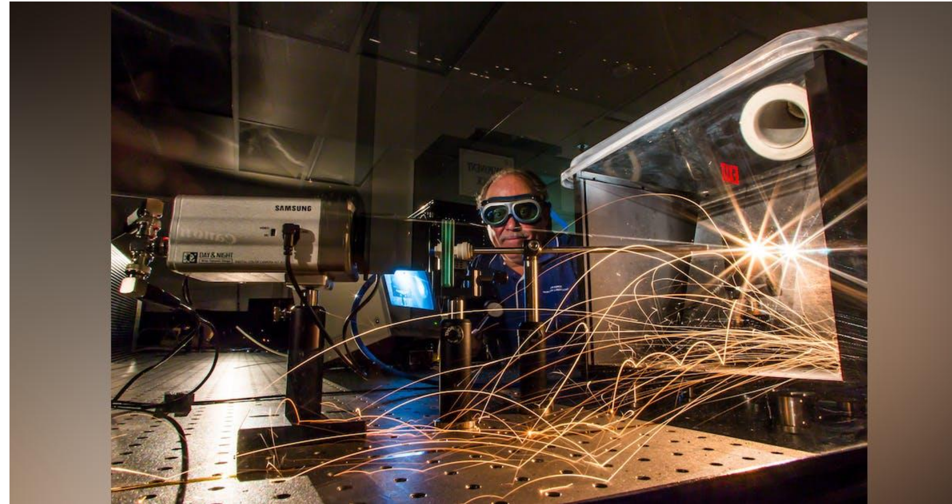
- Undergraduate only
- 20-25 physics majors
- ~20% female
- Recent graduates have gone on to graduate school in Physics, Optics, Physics Education, and Geology, others into industry

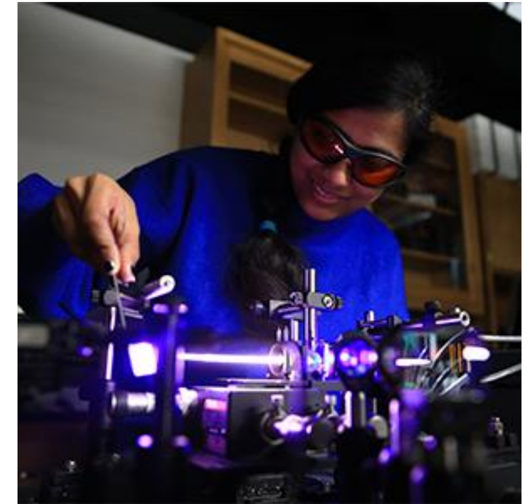
The Department of Electro-Optics and Photonics

- Graduate only
- MS and PhD in Electro-Optics
- ~60 graduate students
- Recent graduates have gone on to academia at places like Brown University and Morehouse College
- Others go to industry like Apple or Intel or go to government labs like AFRL









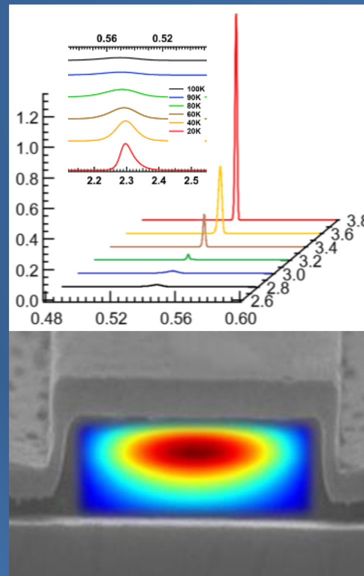
Electro-Optics and Photonics

Dr. Jay Mathews

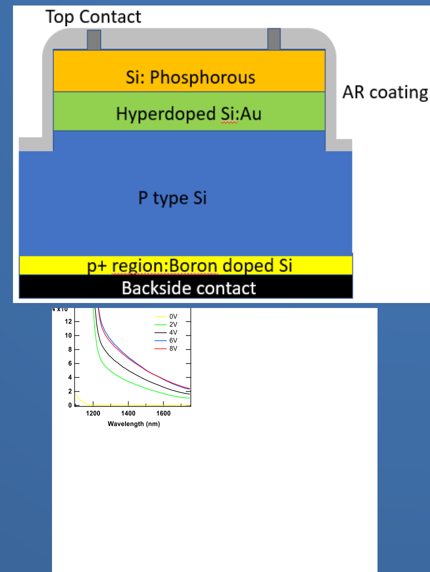
Optoelectronic Materials Lab

Dr. Jay Mathews is an Associate Professor in the Physics department at University of Dayton (UD). Dr. Mathews' research is centered on materials for photonic and optoelectronic devices. His group currently consists of 2 PhD and 2 MS students (Electro-Optics), and 1 undergraduate (Physics). He has active collaborations with Air Force Research Laboratory, US Army Combat Capabilities Command, and Naval Surface Warfare Center Dahlgren, as well as numerous universities. Dr. Mathews has 28 refereed journal publications and has received over $800k in external and internal research funding, and he was a recipient of the 2017 Air Force Young Investigator Award. Dr. Mathews also founded and chairs the Increasing Diversity through Mentored Research (IDMR) Physics Summer Experience at UD for undergraduates from minority-serving institutions, and he received the 2019 Diversity and Inclusion Advocacy Recognition prize from The Optical Society (OSA).

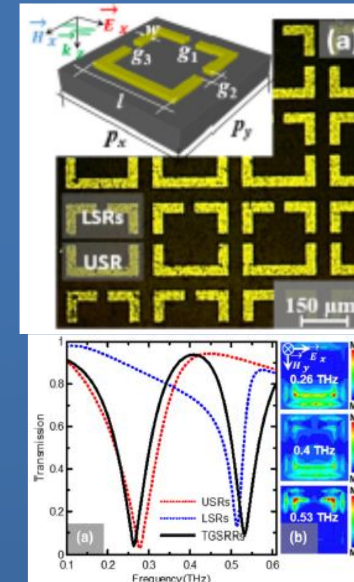
GeSn alloys for IR lasers and detectors



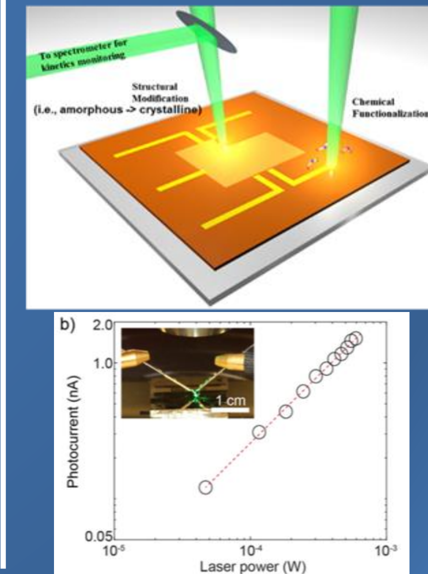
Hyperdoping Si for infrared detection



Metamaterials for THz applications



2D materials for flexible photonics

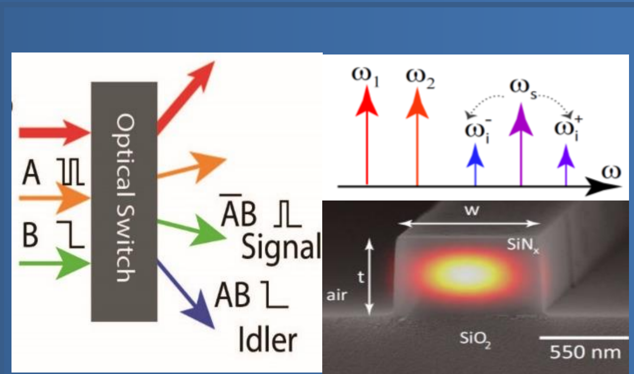


Electro-Optics and Photonics

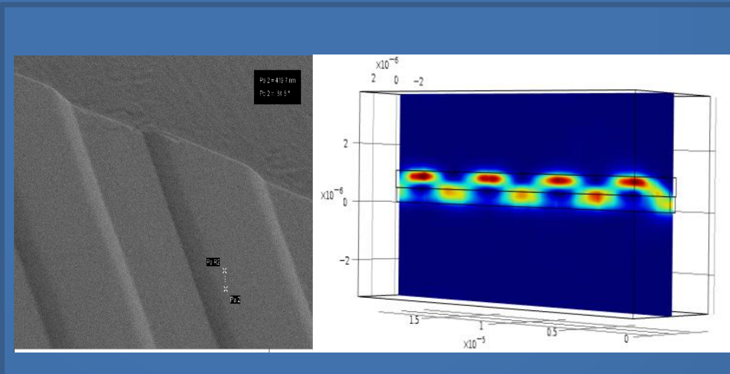
Dr. Imad Agha

Nanophotonics, nonlinear and quantum optics

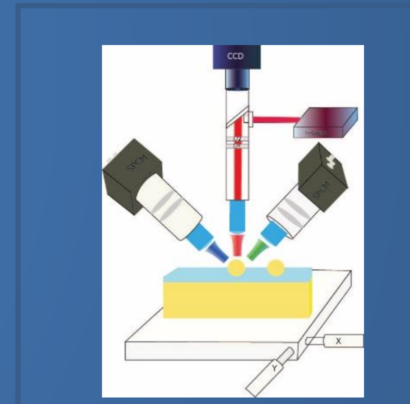
Dr. Imad Agha is associate professor in the Department of Physics and the Department of Electro-Optics and Photonics. He came to the University of Dayton in 2013 after two years as a research associate in the Nanofabrication research group at National Institute of Standards and Technology. His PhD thesis work in nonlinear optics was completed under Alexander Gaeta at Cornell University in 2009, and his postdoctoral work was completed in the group of Philippe Grangier in the Institut d'Optique in Paris. His research focuses on silicon-based micro and nano-photonic integrated circuits, with a vision towards developing transformative technologies in the near future. In his lab, he performs experimental research in silicon-based micro and nano-photonic integrated circuits and phase change materials, developing transformative technologies for the near future.



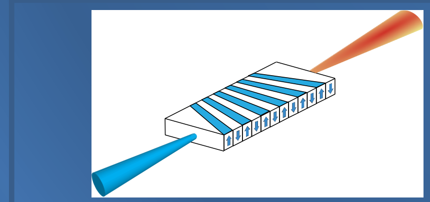
All-optical computing in integrated nanostructures



Thin film waveguides and vertical integration

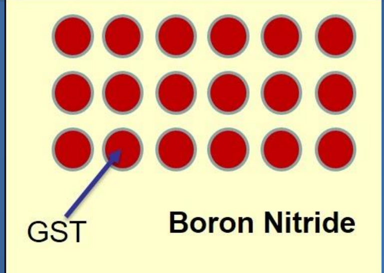


Harmonic generation in nanoparticles



Nonlinear and Quantum Optics: Single Photon Engineering

Phase change materials

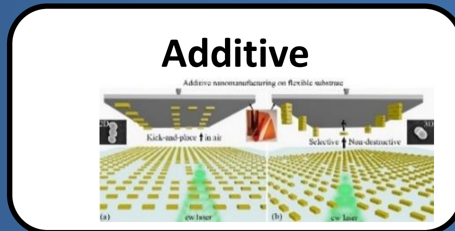


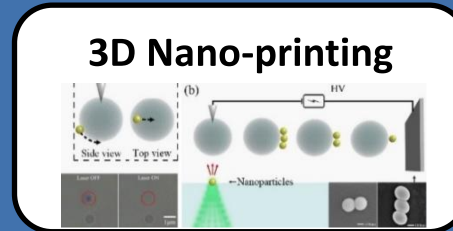
Electro-Optics and Photonics

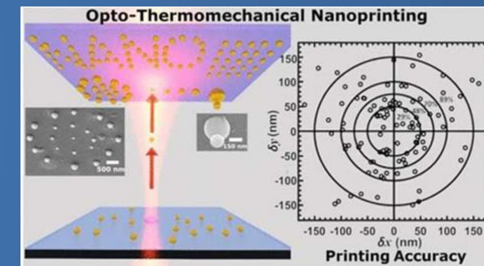
Dr. Chenglong Zhao

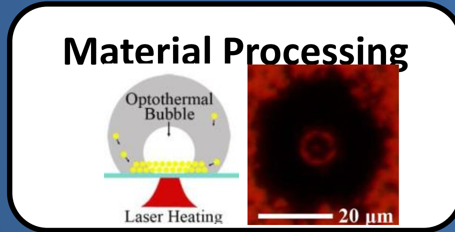
Nano-Photonics & Nano-Manufacturing (NPNM) Lab

Dr. Chenglong Zhao leads the Nano-Photonic & Nano-Manufacturing Lab, which is dedicated to developing cutting-edge nanotechnologies by utilizing the light-matter interaction at nanoscales for applications in additive nanomanufacturing, nanophotonic devices, optical manipulation, and ultra-sensitive optical sensing. Dr. Zhao has authored and co-authored over 20 journal papers including Nature Communications, Nano Letters, ACS Nano, Nanoscale, and Lab Chip. His research findings have been widely reported by Science Daily, Physics News, National Science Foundation, Science Codex, Science News, Nano Werk, etc.

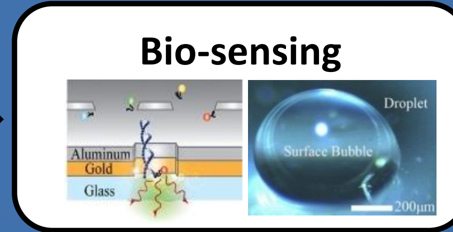




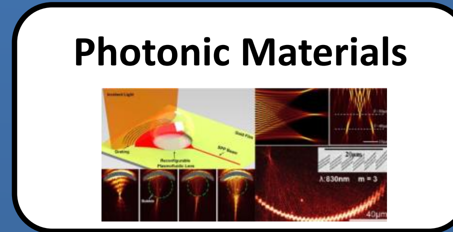




Laser
Photonics
Microfluidics



Work funded by NSF (Zhao, Qiwen Zhan, Ju Shen) to apply data science technology to an advanced manufacturing process for building three-dimensional structures at nanoscale. The process is similar to 3-D printing and uses a laser to assemble 100-nanometer-sized particles on a flexible underlying substrate.



Alam *et al*., Additive Opto-Thermomechanical Nanoprinting and Nanorepairing under Ambient Conditions, *Nano Lett*. (2020)

Electro-Optics

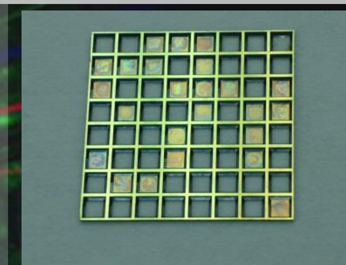
Dr. Andrew Sarangan

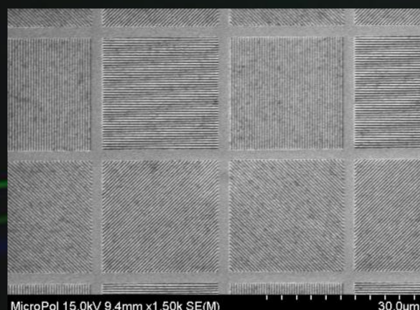
Photodetectors, Thin Films, MEMS, Nano-fabrication

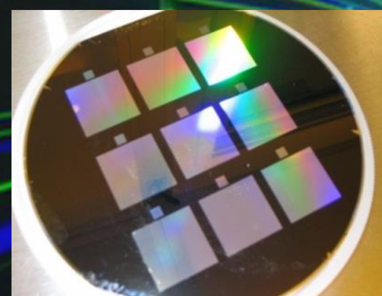
UNIVERSITY of DAYTON

Dr. Sarangan's research includes a wide range of topics in optoelectronics and infrared component design, fabrication and simulation. Examples of his current work include novel concepts in infra-red image sensors, polarimetric sensing, nanostructured thin film based environmental sensors, MEMS packing for optoelectronics integration and manufacturable nano-lithography techniques. He has built and maintains a nanofabrication cleanroom in his lab, and has a number of industry and government partners who contribute to his work. He received the Dayton area Associated Society Council's best researcher award in 2013.

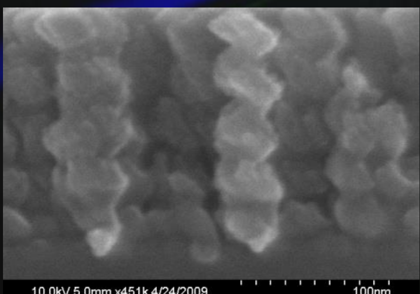
left: transparent metallo-dielectric nano-structures with silver/silica films, *right*: MEMS packaging for UV-photodetectors for medical imaging



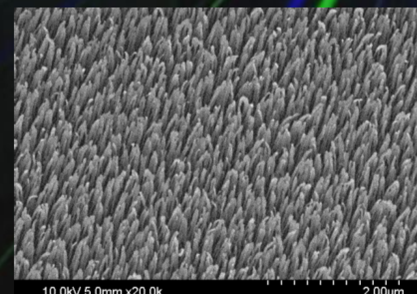




Polarimetric image sensors from wiregrid micropolarizers

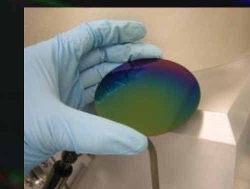


Silica chiral nanocolumns



Silver nanocolumns using Glancing Angle Deposition at cryogenic temps.

Nano-Fab Laboratory
University of Dayton
Prof. Andrew Sarangan

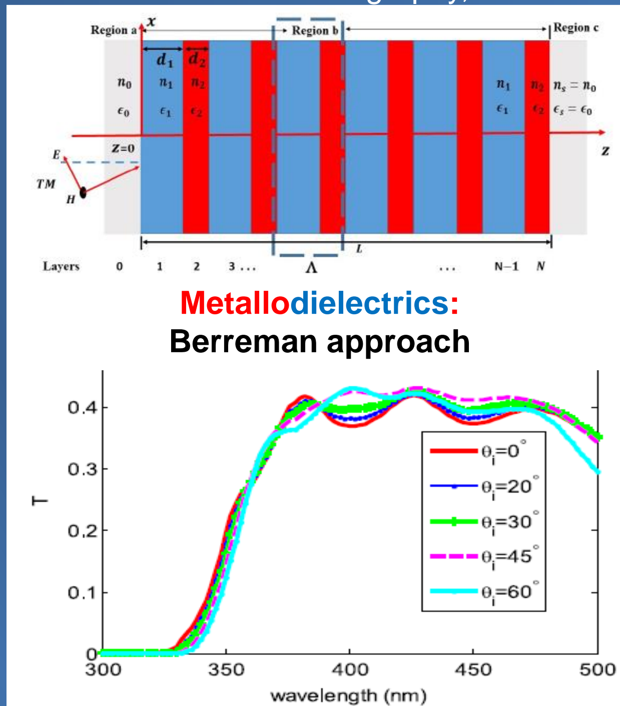


Electro-Optics and Photonics

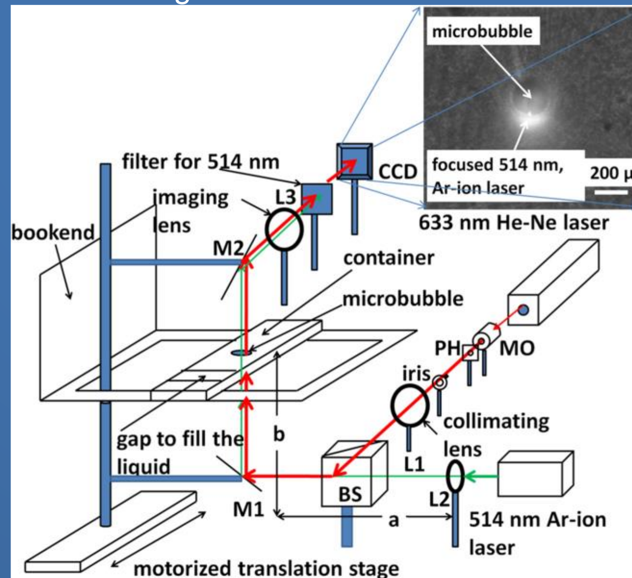
Dr. Partha Banerjee

Digital holography, metamaterials, photorefractives, nonlinear optics

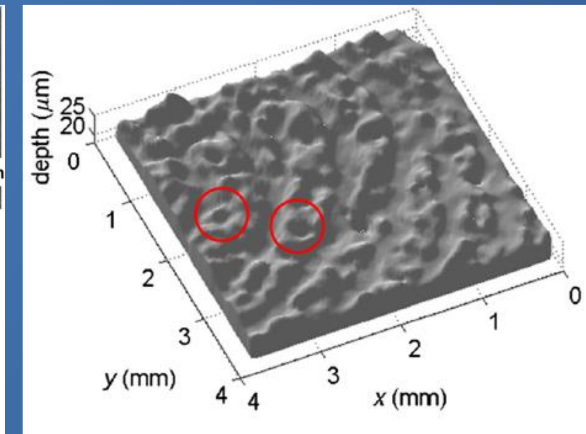
Dr. Partha Banerjee is Professor of Electro-Optics and Photonics at the University of Dayton, where he served as Director and then Chair from 2012-2020. Previously he was also with Electrical and Computer Engineering, where he served as Chair of ECE at UD from 2000-2005. At UD, Dr. Banerjee has established the Holography and Metamaterials lab where he supervises 1 research engineer, 5 PhD students and 3 MS students. He also supervises MS and PhD students who are pursuing their research at Air Force Research Labs, WPAFB, Ohio. He was general chair of OSA's Digital Holography in 2010. 2016 and 2019, and will chair the conference again in 2021. To date, Dr. Banerjee has published 5 textbooks, over 150 refereed journal papers, and over 180 conference papers/presentations, and holds 1 patent. He has supervised over 25 PhD dissertations and 15 MS theses. Dr. Banerjee is Fellow of OSA, SPIE and IoP. He received the NSF Presidential Young Investigator award, the Sigma Xi excellence award, the Dayton area Associated Society Council's best researcher award, as well as the UD Alumni Research Award in 2012. In recognition of his contribution to holography, he received the Holoknight award in 2019.



Metallodielectrics: Berreman approach



Microbubble generation and manipulation using laser beams



3d reconstruction of CTF developed fingerprints using digital holography

OSA DH & 3D Imaging 2021, Vancouver, canada

Electro-Optics and Photonics

Dr. Mikhail Vorontsov

Atmospheric turbulence, high power lasers, additive manufacturing

Dr. Vorontsov is professor and Wright Brothers Institute Endowed Chair with the Department of Electro-Optics and Photonics and director of the Intelligent Optics Laboratory. He has published over 300 papers and four books on the subjects of adaptive optics, atmospheric characterization, beam control, nonlinear spatio-temporal dynamics and image processing. He is fellow of SPIE and OSA and Army Research Lab Emeritus Fellow. He also founded a very successful small company Optonicus, which was recently acquired by II-VI.

Univ Dayton Lab
Optonicus Office
Optonicus Lab

Indoor Range
High Power Laser Material Processing Area
Atmospheric Range
ERASS Lab
Metrology Lab
Wavefront Sensing Lab
Clean Room
High-Power Fiber-Array Lab
Clean Room
Unique Capabilities
Mechanical shop
Electronic shop
Storage room
Fiber – Optics Shop
COO
Office/lab Support
EO Engineers
Computer Engineers
Optical Engineers
Students /Visitors
CFO
Mechanical & Optical Engineers
ITAR Lab DARPA SeaHawk

- High-performance computer (780 processing cores)
- Eight 1.0 kW fiber amplifiers

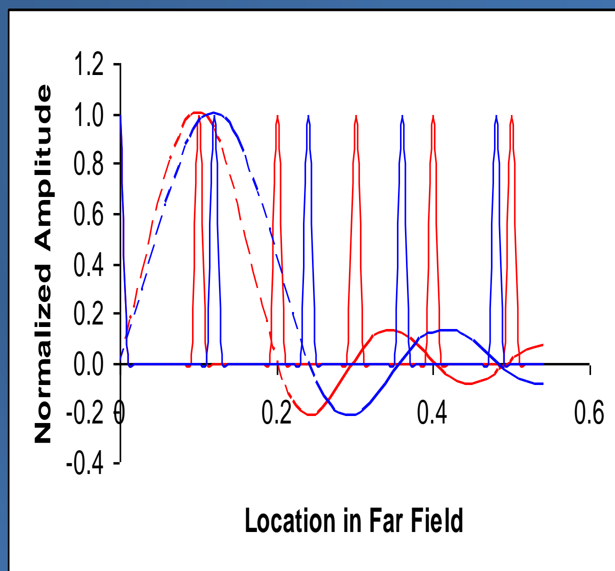
Electro-Optics and Photonics

Dr. Ed Watson

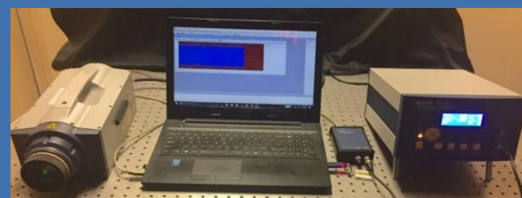
Lidar, Optical Phased Array Technology, Novel Remote Sensing

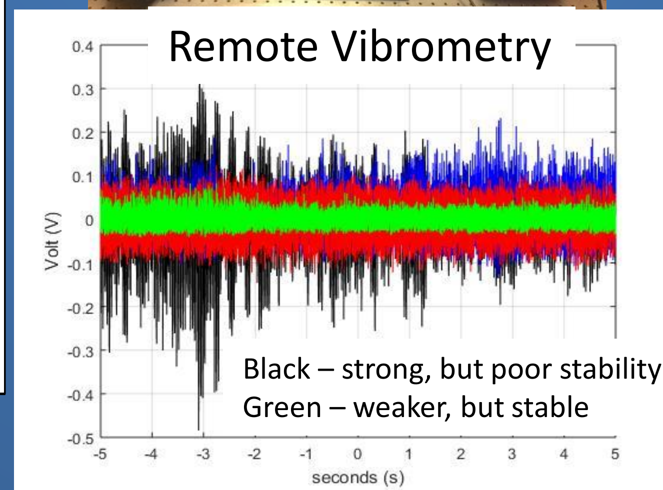
Distinguished Researcher Sensor Technologies, University of Dayton Research Institute. Holds adjunct appointments in EOP and ECE. Chief Executive of Vista Applied Optics, a small optical consulting firm. Retired 2012 from Sensors Directorate, AFRL. Interests include laser radar in its various forms; optical phased array technology; novel remote sensing such as low light level imaging & pattern recognition and speckle characterization. Ph. D. in Optics University of Rochester, M.S. in Optical Sciences and B.S. in Physics from University of Arizona. Fellow of OSA, SPIE, MSS and also an AFRL Fellow. Recipient of the Baker Prize from IEEE and Kingslake Medal and Prize from SPIE.

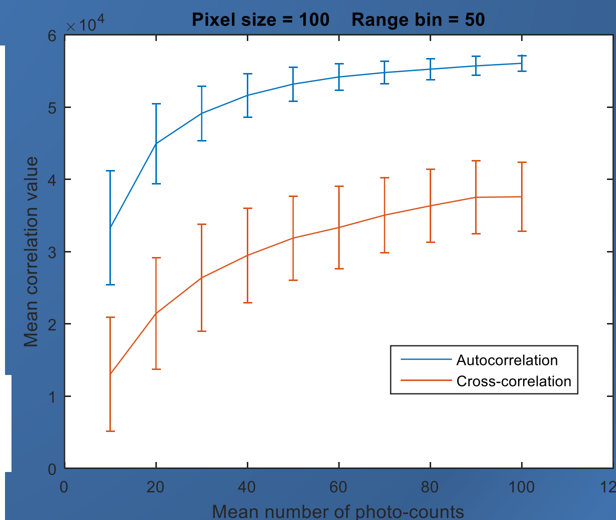
Object Recognition using Low Light Level Imagery



Dispersion of achromatic phase modulator





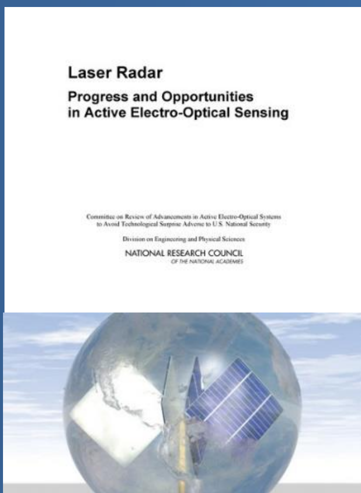


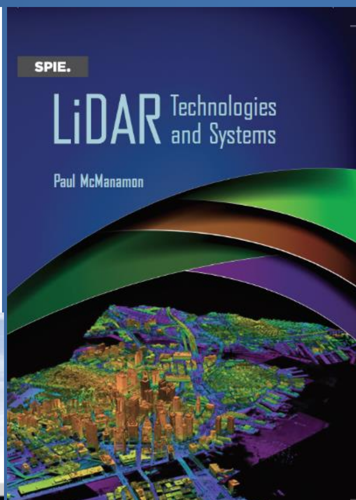
Electro-Optics and Photonics

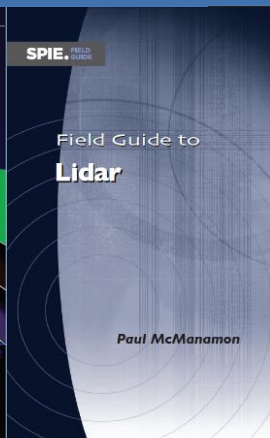
Dr. Paul McManamon

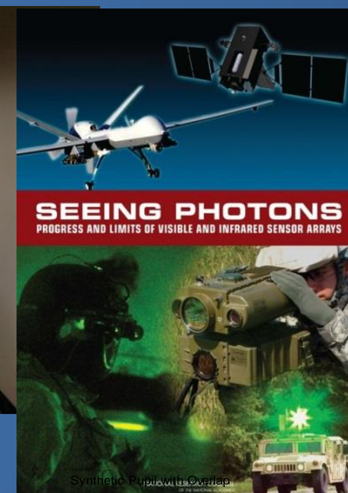
Lidar, Non Mechanical Beam Steering, Spatial Heterodyning, Directed Energy

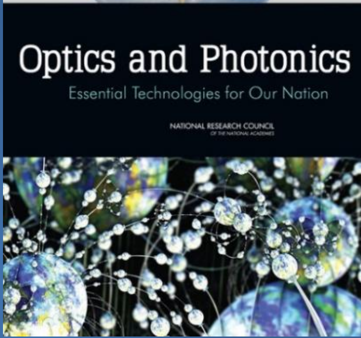
Dr. McManamon's research includes primarily lidar, non mechanical beam steering, Spatial heterodyne, and Directed Energy. Dr McManamon was the 2006 president of SPIE. He is a fellow of SPIE, AIAA, IEEE, OSA, AFRL, DEPs, and MSS. He chaired the 2014 National Academy of Sciences study on Laser Radar. He co-chaired the 2012 NAS study on Optics and Photonics :Essential technologies for our nation, that recommended the National Photonics Initiative, NPI. The NPI has so far resulted in the $610M AIM center, and is working on other initiatives. He was Vice chair of the " Seeing Photons" 2010 NAS study. Dr McManamon was chief scientist for AFRL's Sensors Directorate until his retirement for the Air Force after 40 years as a civilian employee. He has published 2 books on Lidar.

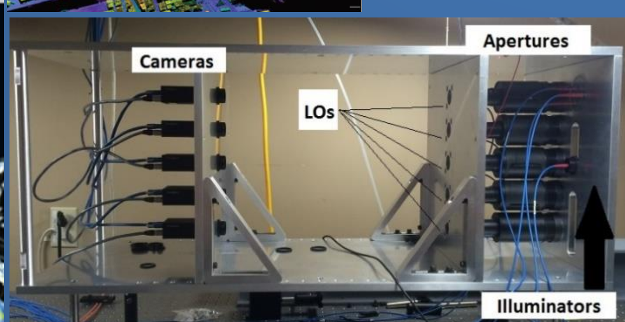


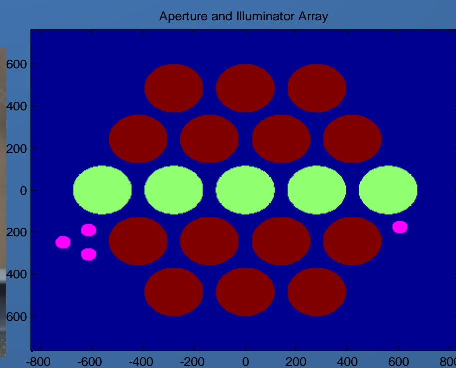


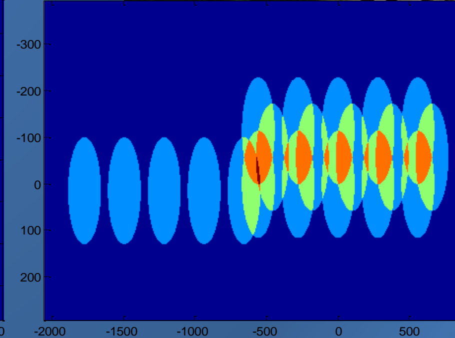












NSF Research Experiences for Undergraduates (REU) Program

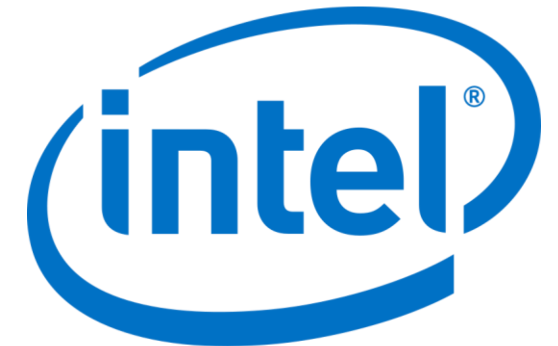
- Paid research internships at colleges and universities
- Usually includes housing and stipend
- Gain research experience under a faculty member

Research Experiences
For Undergraduates

REU Site: Semiconductor Electronics and Photonics at University of Dayton

- 10-week paid internship
- $6,000 stipend
- Housing in UD dorms
- Partial meal allowance
- Subsidized travel to/from site
- Travel funds for presenting at a conference
- Professional development series
- Semiconductor workshop
- Hands-on experience in UD Nanofab Lab
- Semiconductor Rapid Certification: Foundation Level (OASIS, Intel)

Rapid Certification



Application requirements and eligibility

Application requirements

- Application form on Google
- Personal statement (max 750 words)
- Resume/CV
- Unofficial transcript
- Two references

For more info or to apply:

http://go.udayton.edu/reu

Contact: Dr. Jay Mathews
Email: jay.Mathews@udayton.edu

Eligibility

- Enrolled in an undergraduate program during summer 2023
- Science or engineering major
- No minimum GPA
- No knowledge or experience with semiconductors is necessary.
- Applications from minority-serving are encouraged to apply, as are students from underrepresented groups in STEM

Deadline: April 16th

University of Dayton